REMARKS

The specification has been amended to correct errors of a typographical and grammatical nature. Due to the number of corrections thereto, applicants submit herewith a Substitute Specification, along with a marked-up copy of the original specification for the Examiner's convenience. The substitute specification includes the changes as shown in the marked-up copy and includes no new matter. Therefore, entry of the Substitute Specification is respectfully requested.

The abstract has also been amended to more clearly describe the features of the present invention.

Entry of the preliminary amendments and examination of the application is respectfully requested.

To the extent necessary, applicant's petition for an extension of time under 37 CFR 1.136. Please charge any shortage in the fees due in connection with the filing of this paper, including extension of time fees, to Deposit Account No. 01-2135 (501.39484X00) and please credit any excess fees to such deposit account.

Respectfully submitted,

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ABSTRACT OF THE DISCLOSURE

~~[Solution of the Problem According to the Invention] The~~ A reduction of the junction electric field intensity is accomplished in the semiconductor regions for the sources and drains of ~~the~~ field effects transistors. For this purpose, a ~~[Method for Solving the Problem] A~~ structure is provided where the gate electrodes 9 of the MIS•FETQs for memory cell selection of a DRAM are buried within the trenches 7a and 7b created in the semiconductor substrate 1. The bottom corners within the trench 7b are rounded so as to have a radius of curvature in accordance with the sub-threshold coefficient of the MIS•FETQs for memory cell selection. In addition, the gate insulating film 8 within the trench 7b is made to have a laminated structure of a thermal oxide film and a CVD film.

~~[Selected Drawing] Fig. 28~~